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Term	Documents
(30 AND 6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	81
(L30 AND L6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	81

Database: US Pre-Grant Publication Full-Text Database
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side by side			result set
<u>DB</u> =PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; <u>PLUR</u> =YES; <u>OP</u> =OR			
<u>L31</u>	L30 and 16	81	<u>L31</u>
<u>L30</u>	L25 and branch\$5 near6 (predict\$5 or guess\$3 or speculat\$5)	128	<u>L30</u>
<u>L29</u>	L25 and 16	147	<u>L29</u>
<u>L28</u>	L25 and 17	9	<u>L28</u>
<u>L27</u>	L25 and 18	0	<u>L27</u>
<u>L26</u>	L25 and 15	0	<u>L26</u>
<u>L25</u>	hardware near8 (multi or plur\$7 or two or second or multipl\$7) near5 thread\$3	612	<u>L25</u>
<u>L24</u>	(thread\$3 or multi near1 thread\$3) and 11	0	<u>L24</u>
<u>L23</u>	L1 and (machine\$1 or assembl\$4 or compil\$7 or link\$5)	1	<u>L23</u>
<u>L22</u>	L1 and assembl\$4	0	<u>L22</u>
<u>L21</u>	L18 and 18	12	<u>L21</u>

<u>L20</u>	L18 and l7	2	<u>L20</u>
<u>L19</u>	L18 and l6	36	<u>L19</u>
<u>L18</u>	L17 and l5	40	<u>L18</u>
<u>L17</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$ or specif\$5) near8 branch\$5 near6 (predict\$5 or guess\$3 or speculat\$5)	1464	<u>L17</u>
<u>L16</u>	l5 and l3	2	<u>L16</u>
<u>L15</u>	l5 and l2	2	<u>L15</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L14</u>	l2 and l8	4	<u>L14</u>
<u>L13</u>	l2 and l7	2	<u>L13</u>
<u>L12</u>	l2 and l6	17	<u>L12</u>
<u>L11</u>	l5 and l8	17	<u>L11</u>
<u>L10</u>	l5 and l7	9	<u>L10</u>
<u>L9</u>	l5 and l6	92	<u>L9</u>
<u>L8</u>	(712/239)[CCLS]	421	<u>L8</u>
<u>L7</u>	(712/208-213, 233-240)![CCLS]	1366	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	11496	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	(number) near8 instruction\$1 near8 (after or subsequent\$2 or sequnc\$3 or target) near8 branch\$3 near8 execut\$5	162	<u>L5</u>
<u>L4</u>	L3 not l2	4	<u>L4</u>
<u>L3</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$ or specif\$5) near8 branch\$5 near6 guess\$3	28	<u>L3</u>
<u>L2</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$) near8 branch\$5 near6 guess\$3	24	<u>L2</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L1</u>	5724563.pn.	1	<u>L1</u>

END OF SEARCH HISTORY



Search Results

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Results for "((branch* <near/15> (speculat*, guess*, predict*) and number <near/5> instruction")..."

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IEEE JNL IEEE Journal or Magazine

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Article Information:

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

1. Reducing the branch penalty in pipelined processors

Laija, D. J.;

Computer

Volume 21, Issue 7, July 1988 Page(s):47 - 55

Digital Object Identifier 10.1109/2.68

[AbstractPlus](#) | [Full Text: PDF\(780 KB\)](#) IEEE JNL

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

2. SPARC64: a 64-b 64-active-instruction out-of-order-execution MCM processor

Williams, T.; Patkar, N.; Shen, G.;

Solid-State Circuits, IEEE Journal of

Volume 30, Issue 11, Nov. 1995 Page(s):1215 - 1226

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[AbstractPlus](#) | [Full Text: PDF\(1656 KB\)](#) IEEE JNL

3. Control flow prediction schemes for wide-issue superscalar processors

Dutta, S.; Franklin, M.;

Parallel and Distributed Systems, IEEE Transactions on

Volume 10, Issue 4, April 1999 Page(s):346 - 359

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[AbstractPlus](#) | [References](#) | [Full Text: PDF\(716 KB\)](#) IEEE JNL

4. Out-of-order commit processors

Cristal, A.; Ortega, D.; Llosa, J.; Valero, M.;

High Performance Computer Architecture, 2004. HPCA-10. Proceedings. 10th International Symposium 14-18 Feb. 2004 Page(s):48 - 59

Digital Object Identifier 10.1109/HPCA.2004.10008

[AbstractPlus](#) | [Full Text: PDF\(320 KB\)](#) IEEE CNF

5. FSEL - selective predicated execution for a configurable DSP core

Panis, C.; Hirnschrott, U.; Krall, A.; Laure, G.; Lazian, W.; Nurmi, J.;

VLSI, 2004. Proceedings. IEEE Computer Society Annual Symposium on

19-20 Feb. 2004 Page(s):317 - 320

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6. Memory reference reuse latency: Accelerated warmup for sampled microarchitecture simula

Haskins, J.W., Jr.; Skadron, K.;

Performance Analysis of Systems and Software, 2003. ISPASS. 2003 IEEE International Symposium

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7. **Branch classification to control instruction fetch in simultaneous multithreaded architecture**

Knijnenburg, P.M.W.; Ramirez, A.; Latorre, F.; Larriba, J.; Valero, M.;

Innovative Architecture for Future Generation High-Performance Processors and Systems, 2002. International Conference on

10-11 Jan. 2002 Page(s):67 - 76

Digital Object Identifier 10.1109/IWIA.2002.1035020

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8. **Execution-based prediction using speculative slices**

Zilles, C.; Sohi, G.;

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30 June-4 July 2001 Page(s):2 - 13

Digital Object Identifier 10.1109/ISCA.2001.937426

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9. **Two cache lines prediction for a wide-issue micro-architecture**

Shu-Lin Hwang; Feipei Lai;

Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceedings. 6th Australasian

29-30 Jan. 2001 Page(s):71 - 79

Digital Object Identifier 10.1109/ACAC.2001.903361

[AbstractPlus](#) | Full Text: [PDF](#)(1032 KB) [IEEE CFP](#)

10. **Instruction flow-based front-end throttling for power-aware high-performance processors**

Baniasadi, A.; Moshovos, A.;

Low Power Electronics and Design, International Symposium on, 2001.

6-7 Aug. 2001 Page(s):16 - 21

Digital Object Identifier 10.1109/LPE.2001.945365

[AbstractPlus](#) | Full Text: [PDF](#)(524 KB) [IEEE CFP](#)

11. **Prediction and speculation techniques in ILP**

Mitrevski, P.; Gusev, M.; Misev, A.;

Information Technology Interfaces, 2000. ITI 2000. Proceedings of the 22nd International Conference on

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12. **Caching and predicting branch sequences for improved fetch effectiveness**

Onder, S.; Jun Xu; Gupta, R.;

Parallel Architectures and Compilation Techniques, 1999. Proceedings. 1999 International Conference on

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Digital Object Identifier 10.1109/PACT.1999.807575

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13. **Improving trace cache effectiveness with branch promotion and trace packing**

Patel, S.J.; Evers, M.; Patt, Y.N.;

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Digital Object Identifier 10.1109/ISCA.1998.694786

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14. **Control flow prediction with unbalanced tree-like subgraphs**

Toone, B.R.; Franklin, M.;

High Performance Computing, 1998. HIPC '98. 5th International Conference On

17-20 Dec. 1998 Page(s):221 - 227

Digital Object Identifier 10.1109/HIPC.1998.737992

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Casmira, J.; Fraser, J.; Kaeli, D.; Meleis, W.;
Simulation Symposium, 1998. Proceedings. 31st Annual
5-9 April 1998 Page(s):76 - 82
Digital Object Identifier 10.1109/SIMSYM.1998.668444

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29 Nov.-1 Dec. 1995 Page(s):258 - 263
Digital Object Identifier 10.1109/MICRO.1995.476834

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Pnevmatikatos, D.N.; Franklin, M.; Sohi, G.S.;
Microarchitecture, 1993. Proceedings of the 26th Annual International Symposium on
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Pierce, J.; Mudge, T.;
Parallel Processing Symposium, 1994. Proceedings., Eighth International
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Pnevmatikatos, D.N.; Sohi, G.S.;
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